Novel MIC Bipolar Frequency Doublers Having High Gain, Wide Bandwidth and Good Spectral Performance

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ABSTRACT

New high efficiency Bipolar microwave frequency multipliers have been developed having wideband performance, high conversion gain and good spectral properties. Experimental conversion gains of up to 7 dB have been attained for narrow band designs (≈12% BW) and greater than 0 dB for wide-band designs (≥ 40%) at C band. Corresponding fundamental and 3rd harmonic rejections are greater than 45 dBc and 30 dBc respectively. Extensive modeling and computer-oriented design has been employed utilizing harmonic balance.

I. INTRODUCTION

Frequency multiplying circuits find broad application in electronic systems operating in the RF and microwave frequency ranges. Such devices are employed to provide improved design flexibility and transmitter capability in CW, AM and FM transmitter systems and, in the case of low power systems, for application in mixer local oscillators and frequency synthesizers. Low noise frequency multiplication is also highly desirable for modern wideband phase-locked sources for high frequency system applications.

Recently, considerable attention has been focused on the development of high frequency multipliers using GaAs FETs [1-15]. The development of such multipliers is being pursued since they provide the possibility of conversion gain over a broad band of frequencies, have some isolation between output and input terminals, possess good efficiency and consume less power than their diode counterparts. FET multipliers are also investigated because of their potential for lower noise operation, although apparently there has not as yet been a definitive study on this topic [16].

These FET designs feature methods for providing high conversion gain at higher frequencies with typical results (for the fundamental multiplying element) frequently less than 0 dB [1,8,9,13,15], although some designs provide gains of several dB. Except for several special situation designs [5, 10] typical reported bandwidths are on the order of 5-10% with 20% being reported in one case [1]. Unwanted frequency components at the output of multiplier circuits constitute another area of concern which has frequently not been given great attention. Indeed, a perusal of the literature on FET multipliers reveals in many cases, that the rejection of the fundamental frequency component at the multiplier output is frequently not as great as desired.

This paper presents the theory and design of new and unique bipolar frequency doublers which have high gain, wide bandwidth and good spectral performance (i.e. regarding fundamental and undesired output harmonics). The designs feature the use of a bipolar Darlington pair MMIC as the nonlinear element embedded in passive matching networks to provide narrowband designs (5-12%) with up to 7dB conversion gain and wide-band (≥40%) designs with greater than 0 dB conversion gain at C band. These designs possess fundamental and 3rd Harmonic suppressions greater than 45 dBc for the narrowband case and 30 dBc for the wideband case. Extensive computer modeling using Harmonic Balance algorithms was employed in the development of these multipliers.

II. MULTIPLIER NETWORK DESIGN

The basic multiplier network configuration is presented in figure 1. A perusal of this figure reveals that the circuit consists of a microwave bipolar Darlington pair MMIC [17] embedded in matching networks at the input and output ports.

As a prerequisite for achieving an efficient doubler system, a precision nonlinear model was developed for the Darlington pair and harmonic balance simulations [17,18] were employed to arrive at a strategy to best exploit the nonlinear properties of the device to achieve maximum conversion gain. Both simulated and measured results indicated that a short circuit provides the optimum fundamental output termination for maximum conversion gain. However, as a result of the conditional stability of the active device, it is necessary to modify the optimum fundamental termination in order to guarantee less than unity reflection coefficient at the device input. Computer and experimental analysis of the bipolar doubler reveals that the input termination at the second harmonic frequency has a considerable influence on conversation gain. Similar results on input network effects have also been reported for FET doublers [8,14].

A schematic of the bipolar device is shown in Figure 2. By biasing this circuit at moderately low levels (15 to 25 mA) and driving its input with an RF tone on the order of 0 dBm, a partially rectified output current is produced. The output current is approximately the sum of the two dynamic collector currents, although it is found to be dominated by the component from Q2 which has a larger periphery than Q1. The harmonic signals at the device output which are generated as a result of the transconductance nonlinearity of Q1 and Q2 can be enhanced by terminating the device in a low impedance at the fundamental frequency. The low impedance termination results in a steep dynamic load line for Q1 and Q2 which has the effect of peaking the rectified output current.

Output networks were developed which will provide a near optimum (low impedance) termination for conversion gain as well as reject the fundamental and third harmonic components. As alluded to above, a constraint is imposed on the impedance of output networks by the conditional stability of the active

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device. For frequencies below 3 GHz, the active device has a less than unity K factor such that most purely inductively reactive terminations fall in an unstable region of the Smith chart. For this reason an edge-coupled microstrip filter structure was developed for the output network of the narrowband doublers. A short length of transmission line is employed between the active device output and the filter input to rotate the filter impedance trajectory closer to a short circuit in the fundamental frequency band (stopband). A commensurate line length elliptical bandstop structure is synthesized for the input reflector network for the narrowband doubler. The stopband of this network is positioned to reflect the second harmonic signal launched toward the source back toward the active device input where it is subsequently linearly amplified to combine with other second harmonic components at the device output. Harmonic balance simulations have predicted that the doubler conversion gain can be enhanced or degraded by several dB, depending on the phase of the second harmonic reflected from the input network.

III. PERFORMANCE OF EXPERIMENTAL DOUBLERS

Narrow and wide-bandwidth (≈10% and 40% respectively) doublers with output center frequencies of 4 GHz have been developed and fabricated on low loss teflon-fiberglass substrates; input and output networks are composed solely of microstrip elements. One narrow bandwidth design, which employes an input reflector at the second harmonic frequency achieved a flat conversion gain of approximately 3 dB. The wide-bandwidth design, which does not employ an input reflector network, attains a flat conversion gain of approximately 0 dBm. Bandpass structures were used in the output networks for both of the above designs to reduce the fundamental and third harmonic levels at the doubler outputs.

Two versions of the narrowband doubler have been fabricated and tested as shown below (one with and one without the bandstop filter in the input network). Measured and modeled results for the two narrowband designs are presented in Figures 3 and 4. The fundamental and third harmonic levels at the doubler output were greater than 45 dBc for both designs. Note that the conversion gain is higher by roughly 2 dB for the design employing the reflector network. A third design, shown in Figure 5 is seen to achieve a conversion gain of 7 dB by optimizing the distance between the reflector network and the active device input. The output matching network for this circuit is the same as used in the narrowband design of Figure 4. The input network, however, consists of a length of transmission line and a shunt stub. Figure 6 is a photograph of the positive which was used to fabricate the medium band doubler whose performance was shown in Figure 3.

A broader bandwidth (40%) doubler design has been realized by synthesizing a different type of edge-coupled output network [19]. This topology, capable of realizing octave bandwidth, provides a stable, although suboptimum (in terms of conversion gain) output termination for the active device. A simple single stub network has been included on the input of the 40% bandwidth design to improve input SWR. Measured and modeled results for this design are shown in Figure 7 where it is seen that a very flat conversion gain of 0 dB is achieved and fundamental rejection is greater than 30 dBc. Note that in Figure 7, fundamental, second harmonic and third harmonic responses are all plotted on the same graph and that the horizontal scale must be multiplied by the appropriate factor (e.g., the scale reads 3-5 GHz for the second harmonic).

IV. CONCLUSION

Systematic techniques for design of microwave MIC bipolar doublers have been presented. The results are unique in that excellent performance has been achieved in conversion gain, bandwidth and spectral purity. Gains of up to 7 dB have been obtained for narrowband performance (≈10%) and greater than 0 dB for wideband performance (≥ 40%) while fundamental and higher harmonic rejections of 45 dBc and 30 dBc respectively have been achieved.

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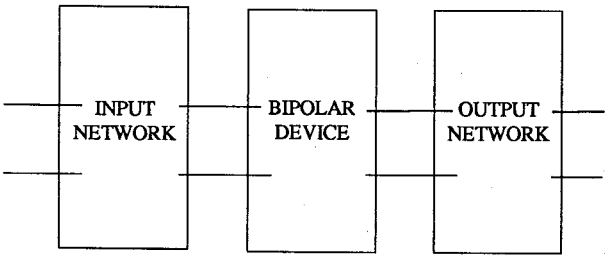

Figure 1. Network configuration

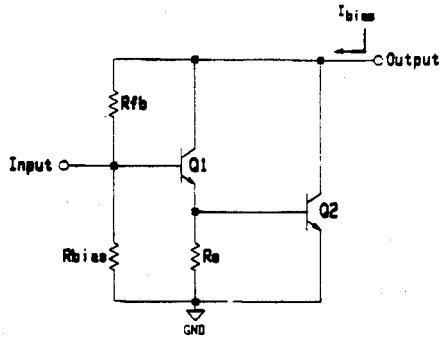

Figure 2. Schematic of Darlington pair used in multiplier application

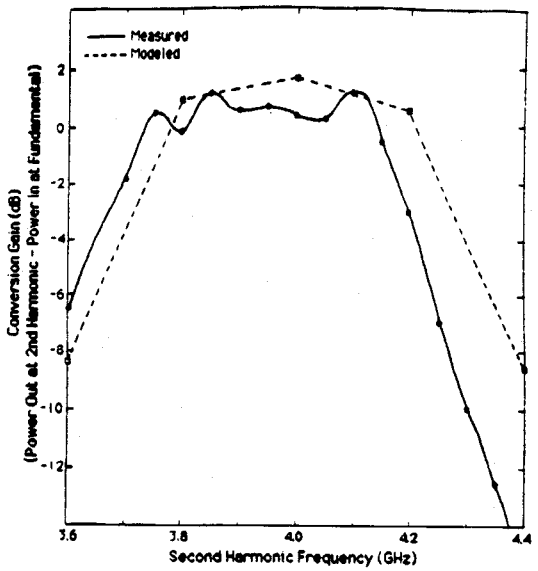

Figure 3. Measured and modeled conversion gain of narrowband coubler without input reflector network (input power = 0 dBm)

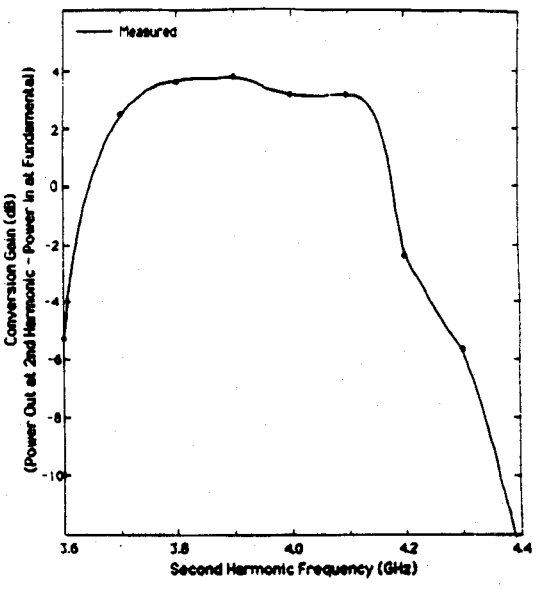

Figure 4. Measured conversion gain of narrowband doubler with input reflector network (input power = 0 dBm)

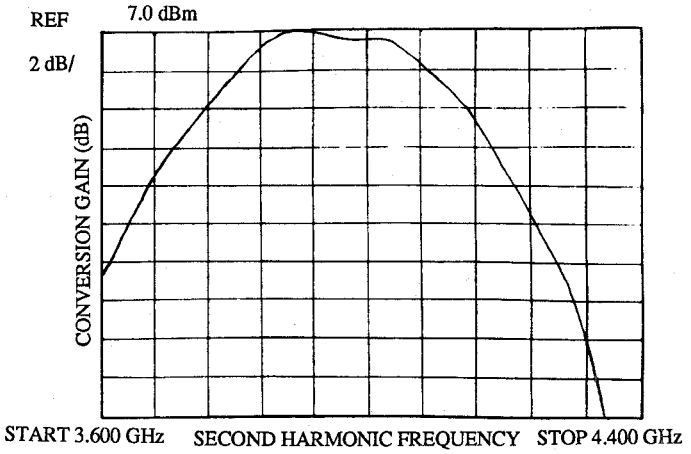

Figure 5. Narrowband design

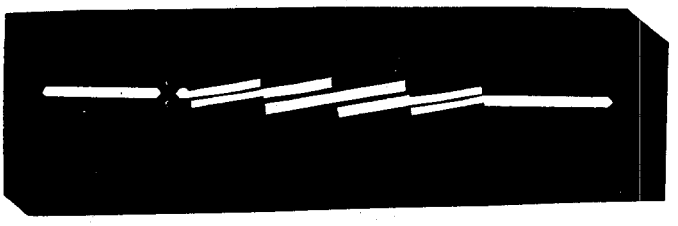

Figure 6. Positive used to fabricate medium band design

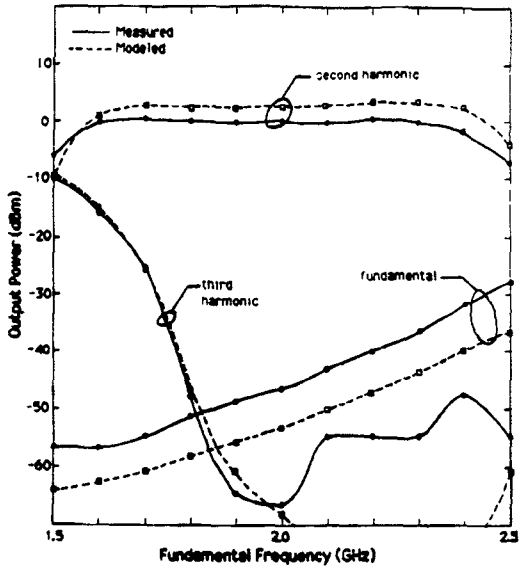

Figure 7. Measured and modeled output power of wideband doubler circuit (input power = 0 dBm)